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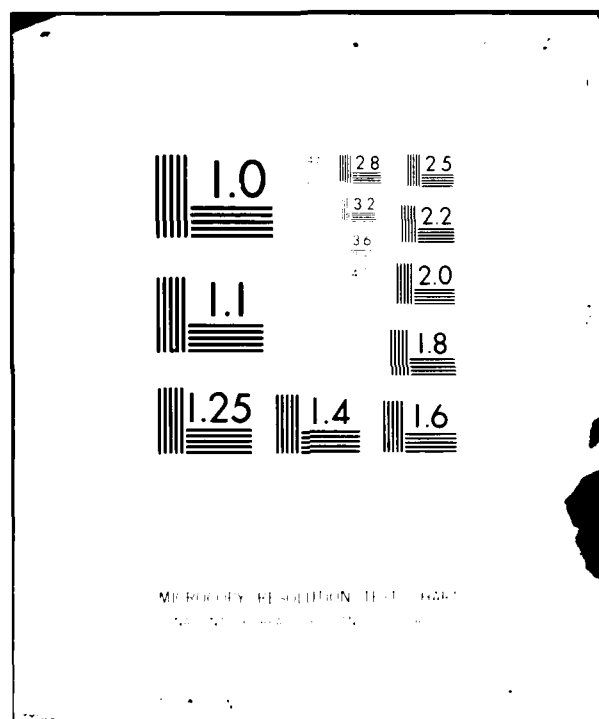
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Final Report
on

Exploratory Studies of Electron Beam
Oxide Densification

AFOSR Contract

AFOSR-80-0088

Principal Investigator: J.C. Wolfe, Asst.Prof.
Electrical Engineering Dept.
University of Houston



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Final Report

on

Exploratory Studies of Electron Beam

Oxide Densification

AFOSR-80-0088

AFOSR Contract [REDACTED]

**Principal Investigator: J. C. Wolfe, Asst. Prof.
Electrical Engineering Department
University of Houston**

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Introduction and Summary

The objective of this study of electron beam densification of deposited oxides was not achieved by the end of the grant period due to unavailability of electron guns from the supplier during this time. The work however was modified and extended to encompass the general area of beam annealing. Several questions of direct interest were investigated experimentally after a general literature survey was completed.

There are two general areas where beam annealing offers potential advantages over conventional furnace annealing. These are annealing of implantation damage and annealing of deposited films for improving density, grain size and stress qualities.

Annealing of implantation damage by electron and laser beams is discussed in detail in Section I of this report. The conclusions may be summarized as follows. It is possible to activate implanted dopant species and anneal implantation damage by pulsed, scanned and multiscanned electron and laser beams. At issue are the questions of activation levels, redistribution of the dopant species and the effectiveness of the process in removing crystal damage. It has been shown that activation levels exceeding the solid solubility limit attained in furnace anneals are possible by beam annealing and that dopant redistribution can be eliminated. It was hoped therefore that scanning methods would improve the performance of fine line VLSI devices where shallow junctions and high activation are required. However, Chu of IBM has recently shown that these super saturated dopant concentrations are unstable against low temperature anneals such as are required in alloy formation of metal contacts and in hydrogen annealing. This fact reduces the interest in this technology substantially because the

contact resistance is then too high for shallow junction devices. These results would not be so serious if it were possible to develop an all-beam annealed technology. This seems to be impossible due to such fundamentally furnace-related technology as hydrogen annealing to eliminate dangling bonds.

The competing technologies, e-beam and laser beam, pulsed, scanned and multiscanned, each have advantages. Pulsed beam annealing produces a uniform dopant distribution up to the junction but does not fully anneal the crystallographic defects in shallow anneals. Scanned and multiscanned annealing does not redistribute the dopant, necessitating a sophisticated ion implant scheme in order to reduce the series resistance associated with the low implanted ion concentration near the surface. However, scanned and multiscanned annealing do a much better job of crystallographic damage annealing than does pulsed annealing. Multiscanned annealing does less damage to oxide vias than either pulsed or scanned beam annealing, has a potential throughput advantage of at least 15 to 1 over single scan methods and does not show the residual effects of the scan lines which even the best single scan annealing exhibits.

Electron beam annealing has an energy efficiency at least three orders of magnitude better than laser annealing and is comparable to furnace annealing (assuming maximum utilization). Moreover, electron beam annealing does not require the delicate control of dielectric film thicknesses that laser annealing does for uniform power absorption.

It is the opinion of the author that multiscanned electron-beam annealing or its functional equivalent is the best of the beam annealing technologies for removal of ion implantation damage and activation of dopant

species. The question of the ultimate utility of any type of beam annealing for this application remains open, however. We are preparing a detailed analysis of this question.

Beam annealing of deposited films for the purposes of densification, stress modification and grain structure modification is currently of strong interest. Stress in SOS devices has been reduced by beam annealing with a concomitant improvement in mobility. Annealing of polysilicon gates and polysilicon on insulator for three dimensional integration has been successful in increasing grain size and reducing resistivity over that obtained in furnace annealing. Pulsed beams are not effective in this area. Scanned beams have shown promise and multiscanned beams have not been tested.

On the basis of the above view of research in beam annealing we decided to study the following questions.

1. Stress in silicide gate structures:

Stress in molybdenum and tungsten disilicide films on silicon was reported by Bell Labs. to be a very serious problem. It was natural to see if stress in silicide gate structures was likewise severe and if beam annealing might be a way to solve the problem. We obtained test wafers from a major semiconductor manufacturer which were prepared as follows: .1 μm silicon dioxide, .25 μm polysilicon and .35 μm of tungsten disilicide were successively deposited on a 4" silicon wafer. The wafers were furnace annealed in dry N_2 at various temperatures and anneal times. Stress was measured in our laboratory. The results are described in Section IV. We found that stress in these films was very low compared to the values reported for silicides on silicon. We therefore saw no reason for studies of ways to reduce the stress.

2. Studies of simulated multiscan annealing:

In multiscan beam annealing, the wafer is thermally isolated and the beam scanned rapidly over the wafer bringing the entire wafer to near the melting point in about 10 seconds. Since the characteristic time of annealing is a few milliseconds and that of diffusion a few minutes, this annealing strategy promotes ion implantation damage annealing without measurable dopant redistribution. Moreover, this strategy avoids completely the scan line overlaps problem, offers a throughput limited only by the loading time of the wafers as compared with 15 wafers per hour in a single scan machine, is energy efficient if done by electron beam and appears to eliminate oxide cracking and rippling as is often observed in single scan machines.

It appeared to us that the characteristic feature of this technique was simply uniform heating of the wafer to near the melting point in a few seconds. Any technique with the characteristic should produce similar results. We hoped to find a cheaper alternative to electron beams. We attempted to simulate multiscan beam annealing with a carbon strip vacuum furnace which we constructed. The program was moderately successful. We showed that some crystallographic defects in furnace annealed material could be removed and that CVD oxide could be densified to furnace annealed quality. The uniformity of heating and the time response of the heating proved to be difficult to control. The process is also energy inefficient compared to furnace annealing. These results are reported in Sections II and III.

In Section V, we briefly discuss our attempts to find a better heating source. These efforts have not yet yielded an improvement over the multi-scanned electron beam. We are still working on this possibility.

I. Comparative Summary of Published Results on Scanned Electron Beam, Scanned Laser and Pulsed Laser Annealing of Ion Implantation Damage in Silicon and of MOS Gate Structures

I.A Introduction

In this review I have compared published work on electron and photon beam processing of ion implantation damage in silicon and MOS-gate structures. Of the various beam heating techniques only scanned electron, scanned laser and pulsed laser beam have been considered. The scope has been deliberately narrowed to give a concise and complete picture of the most promising beam processing technologies and their applications in MOS technology.

I.B Annealing of Ion Implantation Damage in Silicon

I.a. Definitions: There are two broad categories of annealing. These are called "pulsed" and "CW" or "scanned". "Pulsed" annealing takes place by liquid phase epitaxy. "CW" or "Scanned" annealing takes place by solid phase epitaxy. Since rapid dopant diffusion takes place in the liquid phase the depth of the melted zone must be controlled. Typical exposure times are 30 nsec in pulsed annealing. Solid phase annealing requires exposure times of about 1 msec for complete regrowth. Due to the slow diffusion of dopants in the solid phase long exposure times exceeding 10 sec give no measurable diffusion. We use the following abbreviations: Scanned Laser Annealing (SLA); Pulsed Laser Annealing (PLA); and Scanning Electron Beam Annealing (SEBA).

I.b. Doping Profiles: Doping profiles for P, AS, B with PLA show a uniform profile up to the boundary of the molten zone. An example is shown in Figure III.1 (ref. 1). The depth of molten zone is controlled by the

energy of the pulse (2). Other impurities such as Cu and Sb show a zone refined profile with a high concentration near the surface (2). By contrast, CW annealing is characterized by activation of the dopant with little or no redistribution. This has been shown in (3) for SLA and (4) for SEBA. The results have been duplicated in many laboratories. The practical impact of these results is, as shown by Ahmed (4) (Fig. I.2) that a high series resistance exists in SEBA and possibly SLA devices (this has not been shown) due to the low doping concentration near the surface. That this is not the case in PLA devices is seen in Ref. 5.

A dual voltage implant and anneal has been reported (4) to solve this problem.

I.c. Effect of Post-Anneal Heat Treatment on Dopant Activation: Super-saturated dopant concentrations have been reported in all forms of beam heating: in SEBA (6,7), SLA (8,9), PLA (10). Figures I.3 and I.4 show results from Ref. 10 where low temperature heat treatment causes deactivation of As in silicon. Prolonged low temperature anneal leads to precipitation of As and lattice damage.

I.d. Crystallographic Defect Annealing: This is an area where unreliable statements and microscopic deception are present. For example, in an invited paper Williams (11) states, "regrowth from the melt is always perfect". This statement is misleading at best. Great care must be exercised in evaluating the literature.

This aside, one difficulty in pulsed annealing seems to be the difficulty of annealing the tails of the implant damage. Wang et. al. (12) showed that the effect of implant damage tails on diode leakage could be eliminated

only by very deep melting which left the junction depth at 8000 \AA . Campisano et. al. (13) showed that a 450° furnace preanneal of the implant reduces the density of defects in the implant tails (Fig. I.5). This reduces the surface defect density substantially (Fig. I.6). There seems to be agreement that annealing of the tails leads to defect free regrowth, but that unannealed tails serve as seeds for the growth of dislocations (14,15). Since the tails are so deep, this is not a satisfactory solution to the problem for VLSI.

In both laser and e-beam CW annealing, it is advantageous to maintain the wafer at an elevated temperature (16,17). "Defect free" annealing has been reported with lasers (16). Substrate temperatures of $200\text{--}300^\circ\text{C}$ are used to reduce stress. (I would like to comment here that this reported result is probably reliable, but data in this area seems to be fairly sparse.) It is reasonable to expect that better crystallographic defect annealing occurs with the CW over the pulsed mode. This is because a uniform temperature exists throughout the damaged region during the longer exposures characteristics of CW annealing. It should be mentioned, for completeness, that Williams (18) has a far more jaundiced view of defects in CW annealed material (see references in Williams).

I.e. Deep Levels: Deep levels exist in CW annealed materials. They have been ascribed to incomplete damage removal. Johnson et. al. (19) have seen deep level densities up to $10^{15}/\text{CC}$ in self-implanted SLA silicon. Figures I.7 and I.8 show these results. Figure I.7 refers to room temperature annealed material while, in Figure I.8 the wafer temperature was 350°C . These results contrast with the observations of crystallographic defects where the higher temperature eliminates residual damage.

SEBA results Fig. I.9 for As-implanted wafers show similar results (20). These levels occur at concentration up to $6 \times 10^{13}/\text{CC}$, Fig. I.10. What is worse, e-beam scanning of unimplanted wafers induces deep levels, Fig. I.11. These defects occur at densities of $10^{15}/\text{CC}$. The defect distribution is shown in Fig. I.12. Some, but not all, deep levels are eliminated by 450° low temperature heat treatment.

No one has, to my knowledge, studied the deep levels in PLA material. Obviously, this is an area where work is long overdue.

I.f. Annealing of Multilayer Structures: The most obvious difficulty with laser annealing is the sensitive dependence of power absorption on surface films [21], inclusions of damaged material [22], and doping density [23].

The difficulties with inclusions and doping density are not as severe with CW as with pulsed. Oxide thicknesses must be tailored in both cases however (if they are exposed to the beam). In reference 24 it was shown to be possible to successfully tailor both field and gate oxides. Oxide must not be allowed to taper in pulsed work (25) otherwise the doping profile in Figure I.13 results. In reference 26, it was found to be necessary to cover oxide with polysilicon or phosphosilicate glass to prevent cracking under pulsed laser radiation. These problems were reported not to occur by Teng et. al. (27) for SLA.

These problems do not occur with SEBA at elevated wafer temperatures (28).

I.g. Fast Surface States: Fast surface states are induced in e-beam annealing, but these are eliminated by a hydrogen anneal (29).

I.h. Scan Line Overlap Problem: Scanning is required in each of the technologies SLA, SEBA, PLA. The problem of getting uniform coverage is very difficult to solve. In SLA, Mizuta (38) shows that electronic defects remain in material which is free of crystallographic defects. This is shown in Figure I.14 where diode collection efficiency shows clearly the effect of scanning even under optimum conditions of slow scan and large overlap. In PLA, the problem is worse. Kaplan et. al. (30) show results where the scan lines are clearly visible.

One interesting approach to this problem is multiscan annealing (17,37), where the beam is scanned repeatedly over the wafer surface bringing the entire wafer to near the melting point in a few seconds. Device results with a multiscanned electron beam are excellent. Laser results have not been reported. It would be more difficult with lasers because heat conduction of air would cause non-uniform heating and because oxidation may become important in the longer time frame. Clearly a large area beam would be useful.

I.i. Beam Uniformity: Beam uniformity is a big problem in PLA. The "Cullis Homogenizer" is used to improve the situation (31). It is not a problem in SEBA or SLA.

I.j. MOS Devices: There are two reports of MOS transistors fabricated by SLA (27) and PLA (26). In the PLA results, the oxide needed to be protected from the beam by poly or thick phosphosilicate glass. This was not required in SLA samples. It was possible to anneal through the 350Å gate oxide covering the source-drain region in SLA. In the PLA results, this oxide was removed. The source-drain breakdown voltage was "better" in SLA

than in PLA. The diode I.V. characteristics in SLA samples was the same as in furnace annealed samples. The sheet resistance of the poly was $22\Omega/\square$ as opposed to $25\Omega/\square$ in the furnace annealed poly. The furnace annealed poly had a $.3\ \mu\text{m}$ grain size whereas the SLA poly has a $1\ \mu\text{m}$ grain size. Source and drain sheet resistivities in PLA annealed samples were $20\Omega/\square$ with only a $.25\ \mu\text{m}$ junction depth. SLA results were not reported.

McMahon and Ahmed (17) have reported excellent bipolar results with no oxide cracking by multiscan and scanned e-beam. No MOS transistors have been reported by SEBA.

In summary, the many potential problems to device performance related to crystallographic defect, deep levels and scan lines have not been observed. The critical yield study has not been reported.

I.k. Annealing Gate Structures: The main objective in poly annealing is to increase the grain size, thereby increasing the mobility. This is best done by CW techniques. Grain sizes larger than $1\ \mu\text{m}$ have been reported (32,3,30). Grain sizes of $1000\text{--}2000\ \text{\AA}$ have been reported for pulsed annealing (33,34). However, since furnace annealing produces grains of $.3\ \mu\text{m}$ (30), these results are not spectacular. Sheet resistivity of $25\Omega/\square$ for furnace annealed poly is reduced to $20\Omega/\square$ for SLA poly with the same doping level.

Silicide annealing is very poor in the pulse mode (35). Cellular structures form and the metal concentration is non-uniform. However, SLA can be used (36) to nucleate single phase films of Pt, Pd, Nb sillicides. No results have been reported on Mo or W sillicides.

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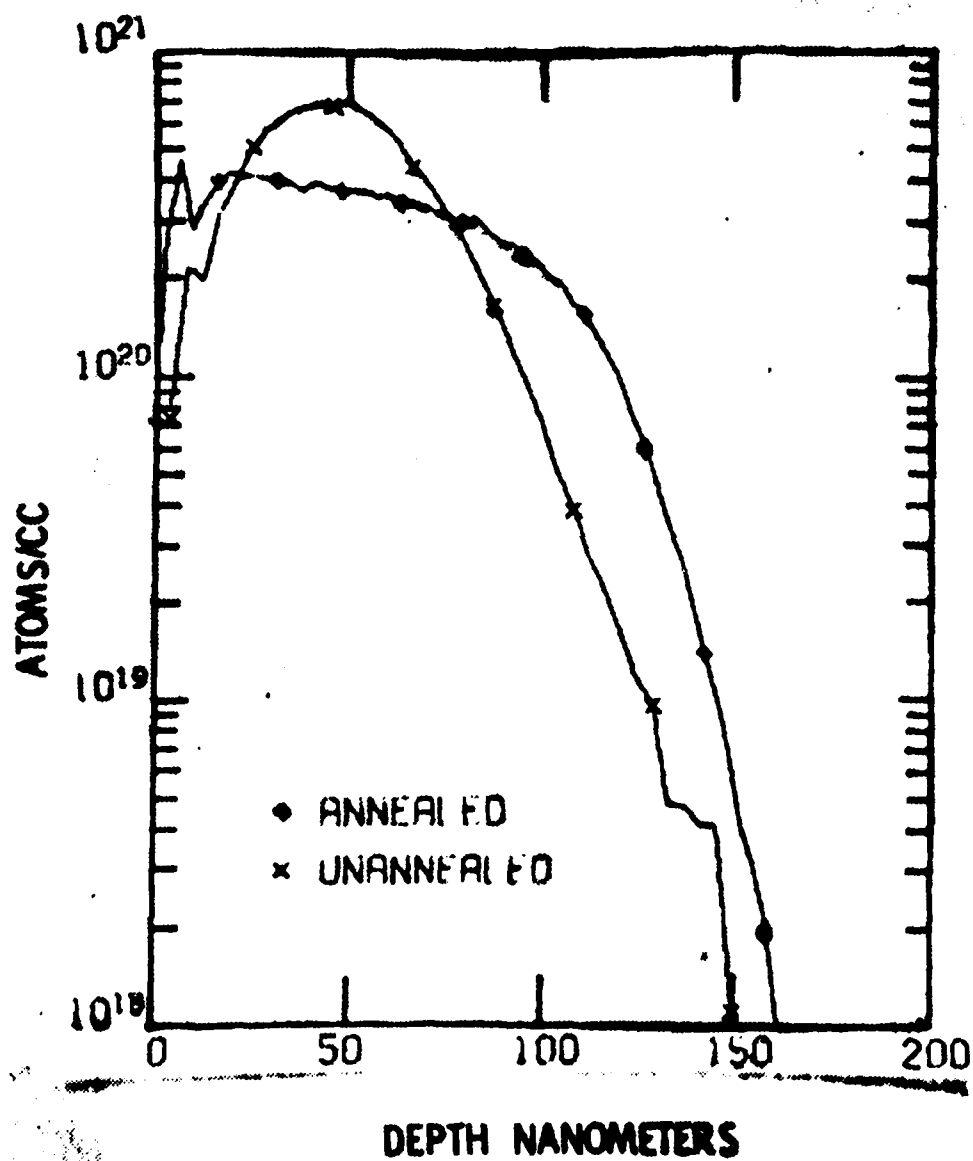


FIGURE I.1 REFERENCE 1

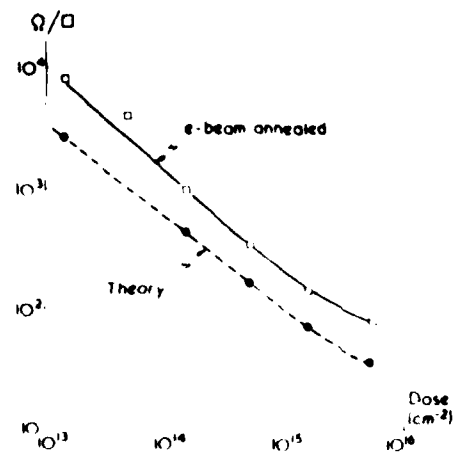


Fig. 1 Sheet resistivity as a function of dose for e-beam annealed As implanted Si (100keV, 10^{13} - 10^{16} /cm²) compared with the predicted resistivity of fully activated material.

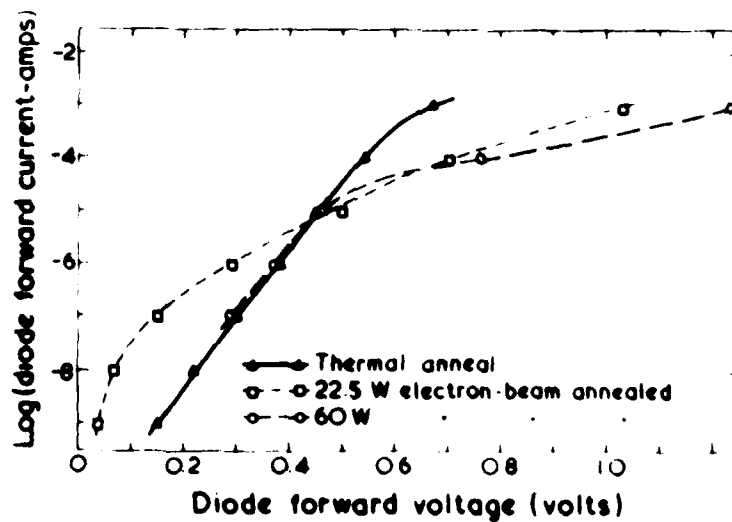


Fig. 2 Comparison of the forward characteristic of p-n diodes annealed with different e-beam power levels and by a standard thermal anneal.

FIGURE 1.2 REFERENCE 4

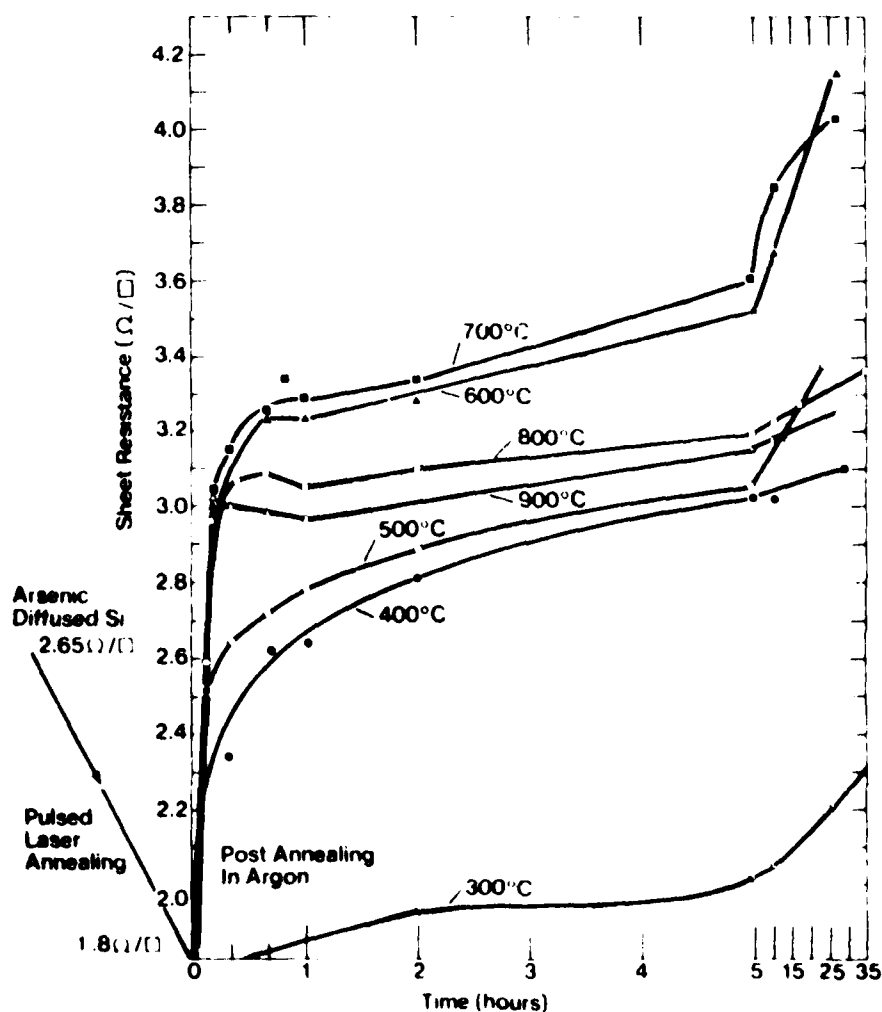


FIG. 1. Sheet resistance measurements on samples of 1050 °C As-diffused Si before and after laser annealing and isothermal annealing of laser-treated samples. (Scale condensed between 5 and 35 h.)

FIGURE 1.3 REFERENCE 10

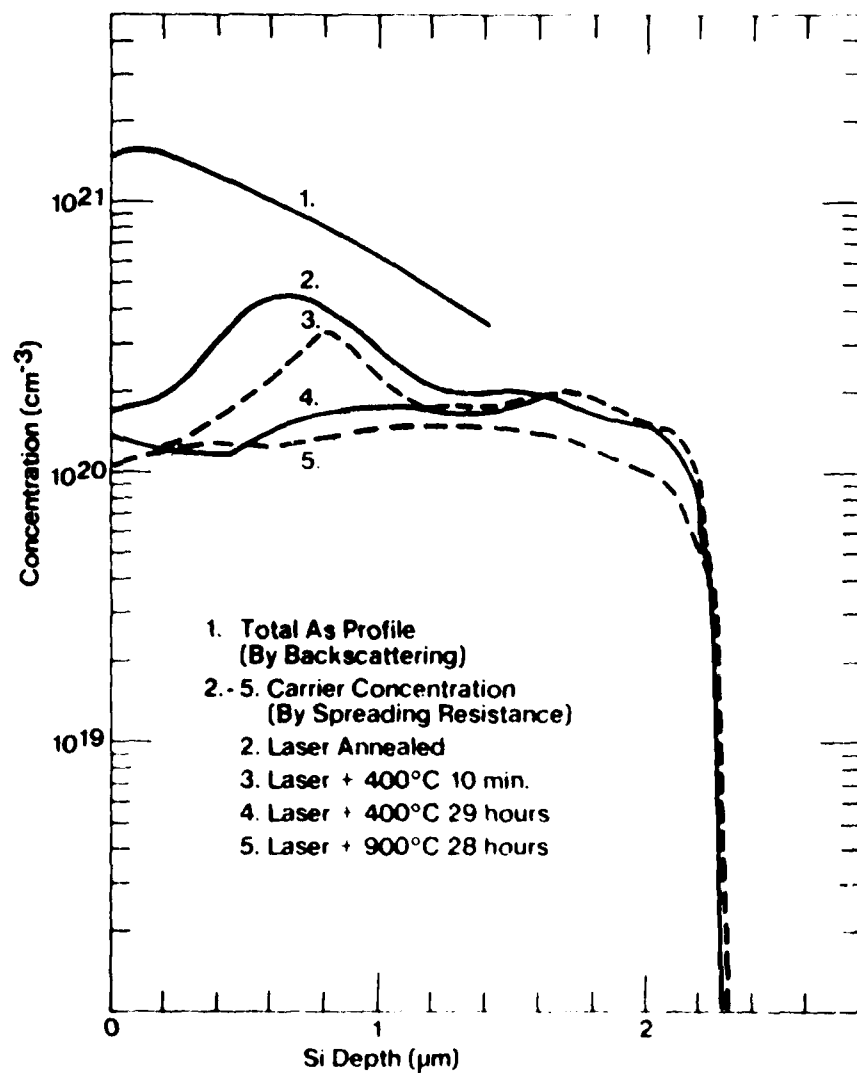
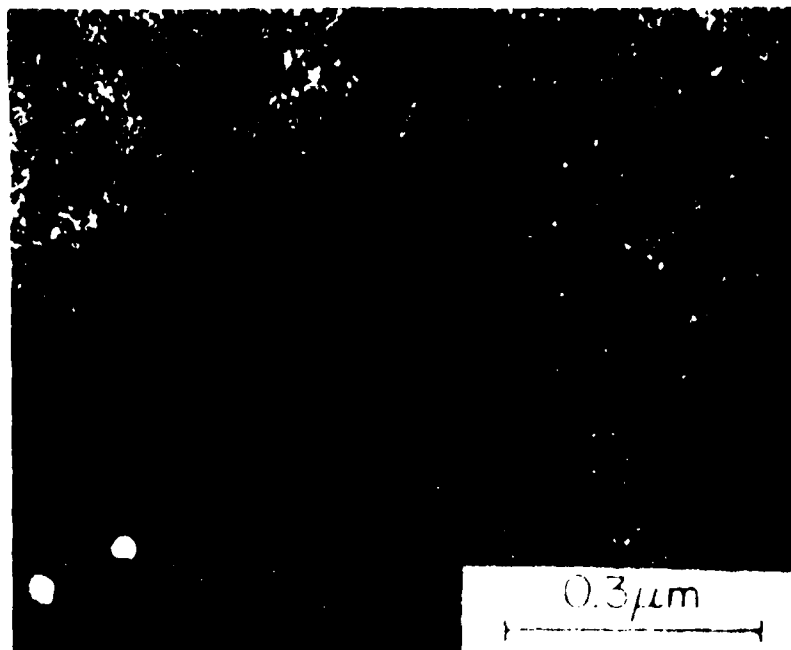


FIG. 2. Total As and carrier concentration profiles of various annealing conditions.

FIGURE 1.4 REFERENCE 10



(a)



(b)

FIG. 5. (a) Top left corner of Fig. 11. Micrograph of the surface after 4500 A anodic oxide stripping. (b) An enlarged view of the surface after anodic treatment at 4500 A. (c) Same as (b).



(a)



(b)

FIG. 2 (a) Dark-field micrograph showing intrinsic stacking fault tetrahedra in PA sample after 2.0 J/cm^2 irradiation. (b) bright-field micrograph showing intrinsic faults in as-implanted sample after 2.5 J/cm^2 irradiation

FIGURE 1.6 REFERENCE 13

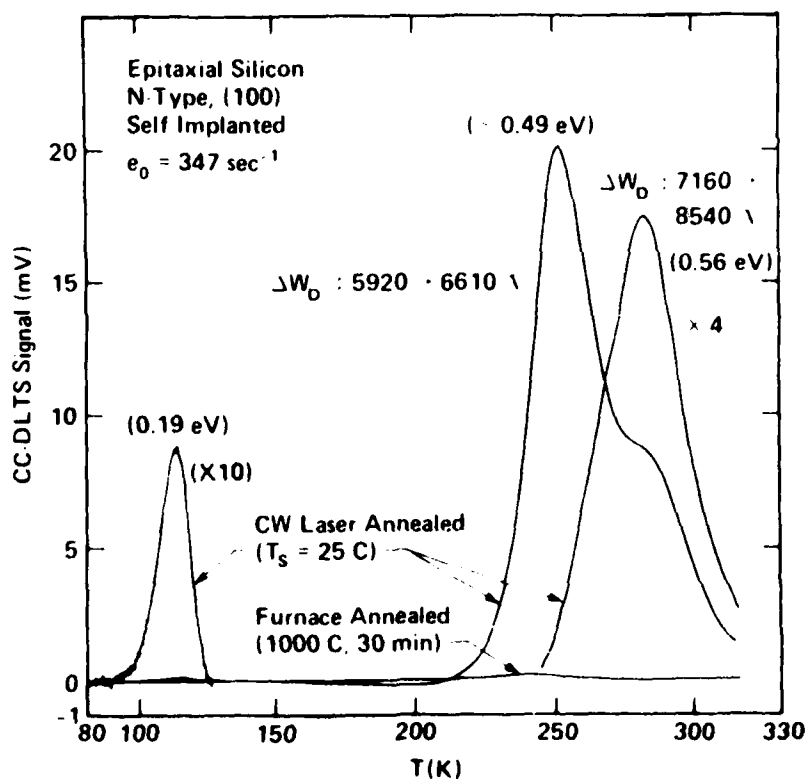


FIG. 1. CC-DLTS spectra for electron emission in self-implanted cw laser-annealed silicon and in a furnace-annealed control device.

FIGURE I.7 REFERENCE 19

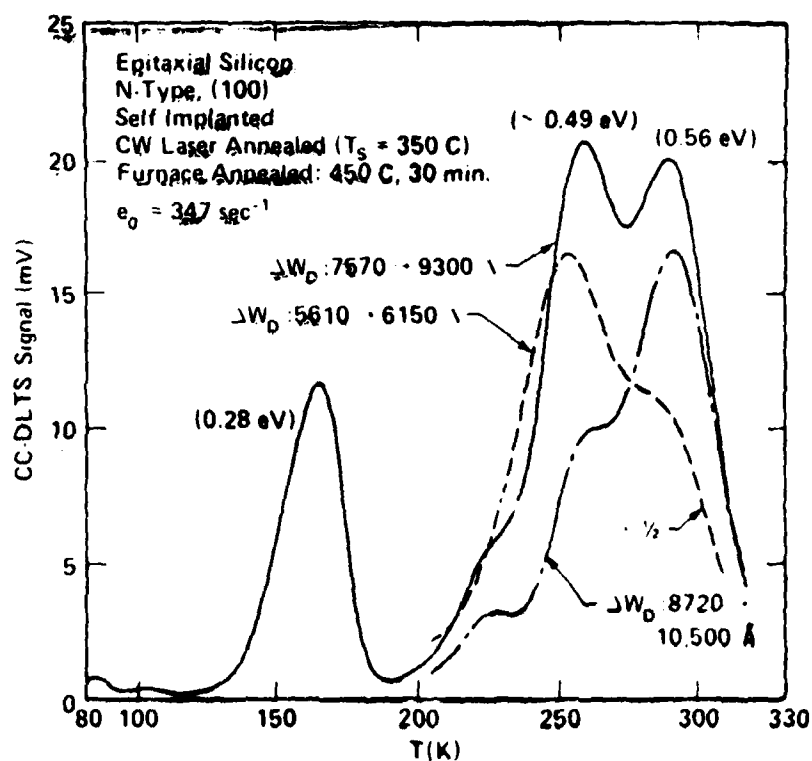


FIG. 2. CC-DLTS emission spectra for a self-implanted laser-annealed diode which also received a 450 °C furnace anneal.

FIGURE 1.8 REFERENCE 19

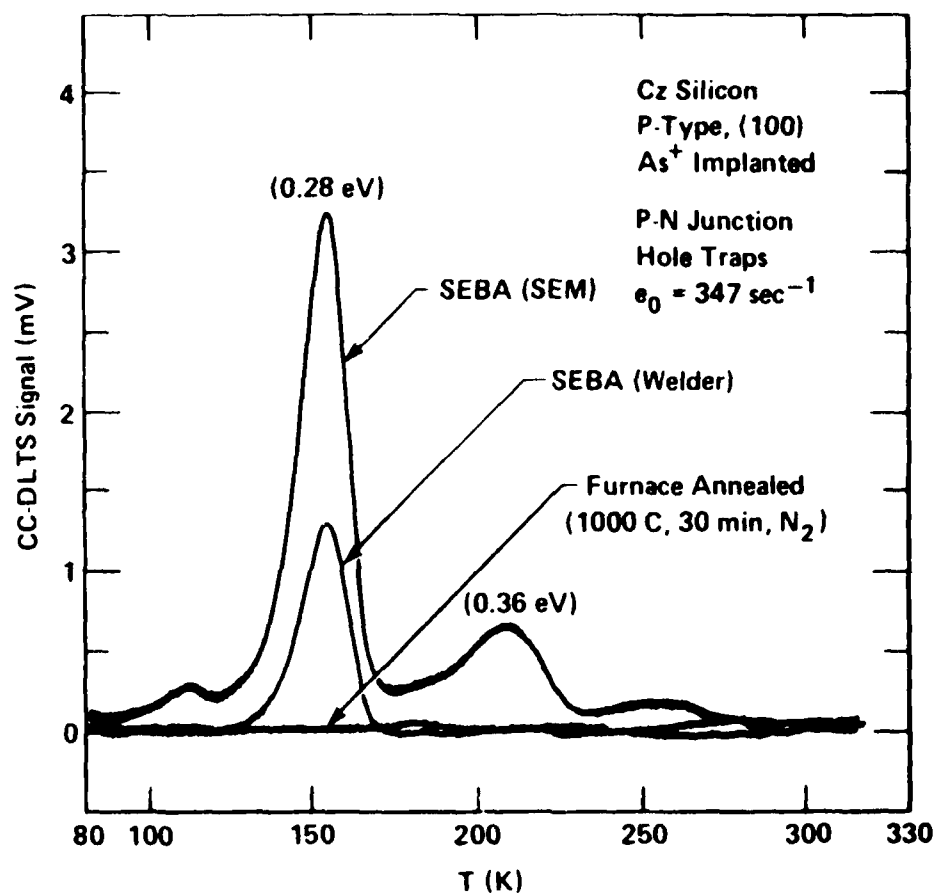


FIG. 1. CC-DLTS spectra for hole emission in As⁺-implanted scanned electron-beam annealed silicon. The spectrum for a furnace-annealed *p-n* junction diode is also shown.

FIGURE 1.9 REFERENCE 20

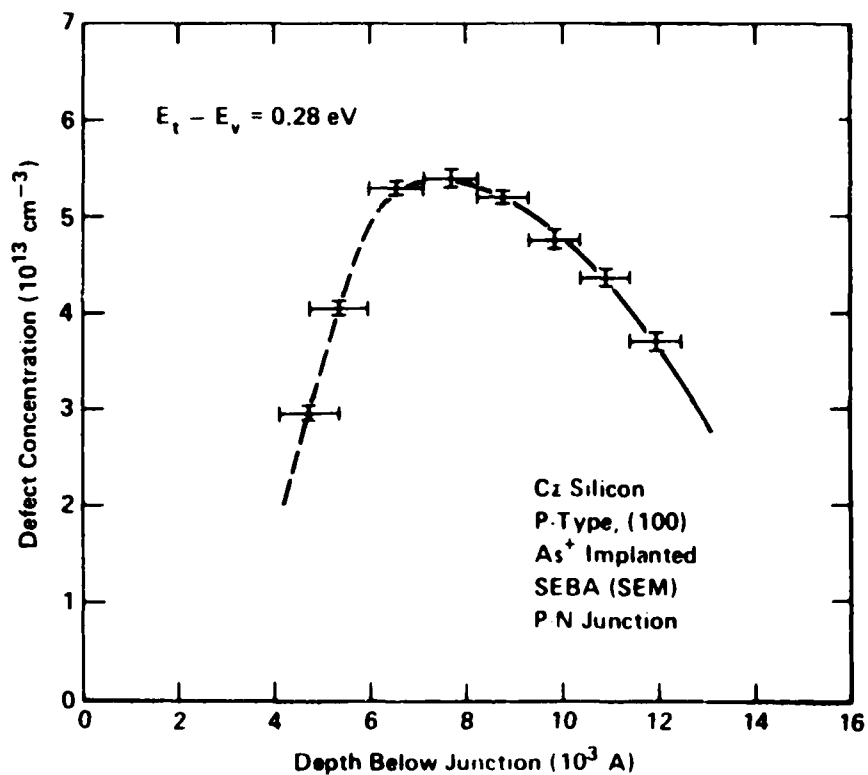


FIG. 2. Spatial depth profile of the defect level at $E_t + 0.28 \text{ eV}$ in As^+ -implanted scanned electron-beam annealed silicon.

FIGURE 1.10 REFERENCE 20

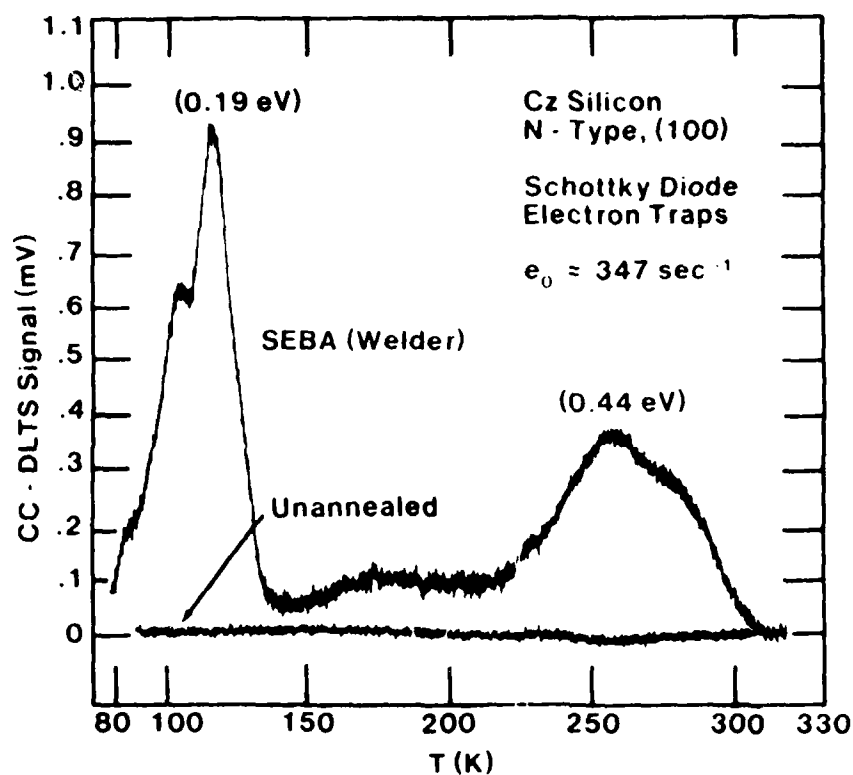


FIG. 3. CC-DLTS spectrum for electron emission in unimplanted scanned electron-beam annealed silicon. Also shown is the spectrum for the unannealed material.

FIGURE I.11 REFERENCE 20

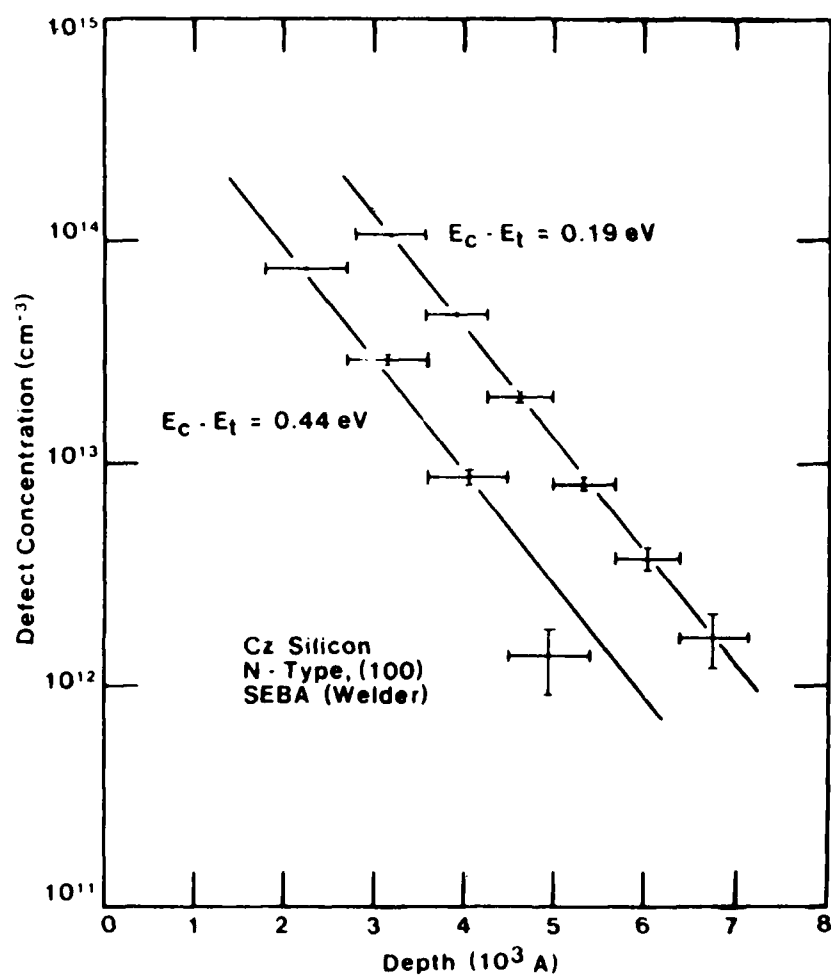


FIG. 4. Spatial depth profiles of the defect levels at $E_c - E_t = -0.19 \text{ eV}$ and $E_c - E_t = -0.44 \text{ eV}$ in unimplanted scanned electron-beam annealed silicon.

FIGURE I.12 REFERENCE 20

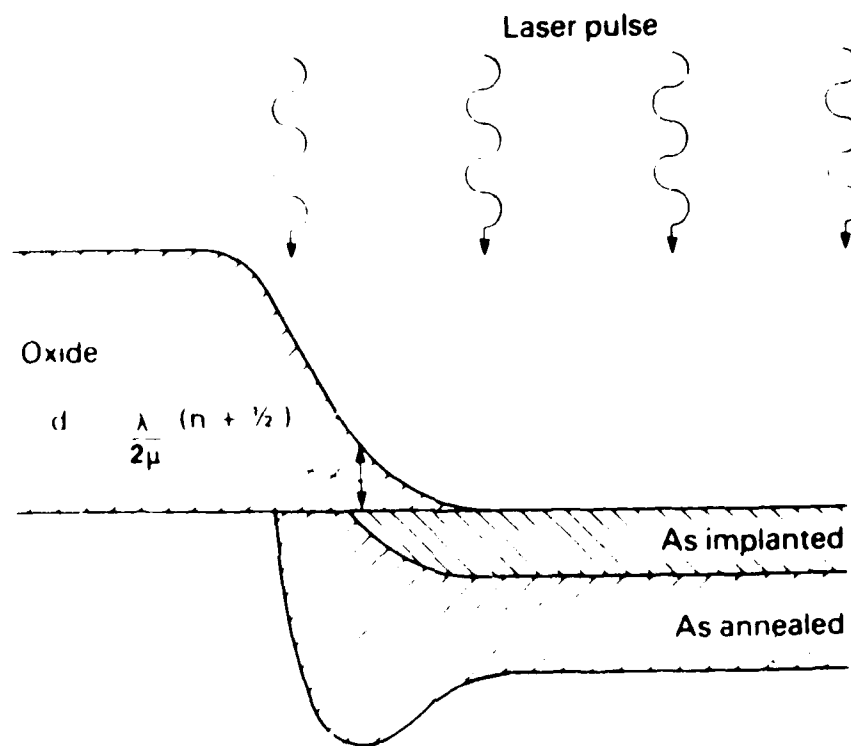


Fig.3. Schematic section through implant window edge showing enhanced optical energy absorption caused by the anti-reflection properties of the oxide mask.

FIGURE I.14 REFERENCE 25

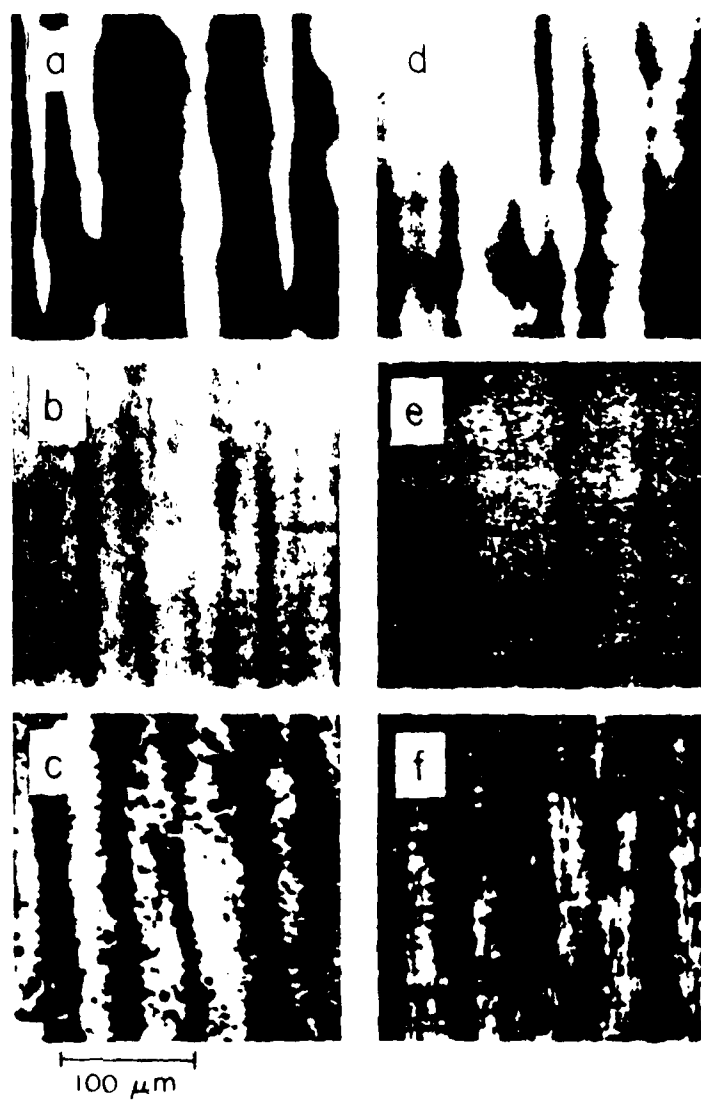


FIG. 2. EBC micrographs for (b)-(f). As shown, the specimen was a 100 μm spot in a 1 μm step. The electron beam was 10 kV and the power was 100 W. The electron beam was 10 kV and the power was 100 W. The electron beam was 10 kV and the power was 100 W.

FIGURE 1.15 REFERENCE 38

II. Preliminary Studies of Crystallographic Defects in Silicon Wafers Annealed by the Simulated Multiscan Method

A series of experiments were undertaken to explore some questions related to heating of silicon wafers to temperatures approaching the melting point for times on the order of seconds to minutes. As explained in the introduction this experimental regime is relevant to multiscan e-beam and laser annealing of silicon.

The wafers were heated in vacuum using a carbon strip heater (as described by Geiss (1)) in contact with the wafers. This furnace was capable of melting the wafers in about 10 seconds. Temperatures were measured using an optical pyrometer. The temperature distribution was relatively uniform over an area of 1 cm \times 1 cm. Temporal control of the temperature was however rather poor. Further work should have a control system involving an automatic pyrometer. Difficulty was encountered in determining the exact temperature due the fact that the light from the carbon strip would reflect from the silicon. Thus, it was difficult to differentiate the carbon strip temperature from the wafer temperature.

Crystallographic defects were studied with the Wright etch (2). Wafers were cleaned prior to etching by the following procedure.

1. Dip for 1 minute in 50:1 $H_2O:HF$
2. Rinse
3. Boil 10 minutes in 1:1 $H_2SO_4:H_2O_2$ (30%)
4. Rinse

Etching was done at room temperature. The etch rate was assumed to be 1 $\mu m/min$ (2).

The wafers for study were generously supplied by a major semiconductor

manufacturer. The wafers were covered with 1 μm of "Silox" oxide and had been furnace annealed in N_2 at 950°C for 1 hour.

A baseline was established by etching the wafers without any further heat treatment.

The maximum defect density was observed after a 1 minute etch to a depth of about 1 μm . The average size was 5 μm . These are shown in the SEM micrographs (Figures II.1,2,3).

Wafers from which the oxide had been removed exhibited severe surface damage when rapidly heated to temperatures as low as 950°C. The SEM micrograph (Figure II.4) shows the surface damage to a silicon wafer heated to 1200°C in about 5 minutes.

Surface damage could be avoided if the wafers were oxide coated during the heating process. Moreover, many of the smaller defects in the silicon were removed by heating. Figure II.5 is an optical micrograph of a furnace annealed sample which had been etched to a depth of 10 μm . Note the high density of small defects.

Figure II.6 illustrates the effect of annealing. The sample was heated close to the melting point (1250-1400°C) for 1 minute. It has been etched to 10 μm . The larger defects remain, however the smaller ones have been removed.

Discussion: In these experiments, the wafers were heated by conduction from a resistively heated carbon heating element in vacuum. Thermal contact is always poor in vacuum and wafers larger than 1 cm \times 1 cm could not be heated uniformly. A similar series of experiments were conducted wherein the wafers were heated by radiation from the carbon heater. It was found that sufficient power absorption was not obtained to raise the temperature

to the extreme values desired. A more efficient means of energy transfer to the wafer than by thermal conduction or radiation is very desirable. Electron beam heating, as Ahmed (3) has shown, would therefore appear to be ideal because high uniformity and efficient energy absorption can be realized.

It has been shown, however, that it is possible, not only to heat silicon wafers to near the melting point in short times without damaging the crystal structure, but that this treatment actually improves upon conventional furnace anneals.

Surface damage has been observed in wafers which were heated without an oxide coating to comparatively low temperatures. The reasons for this behaviour require further investigation.

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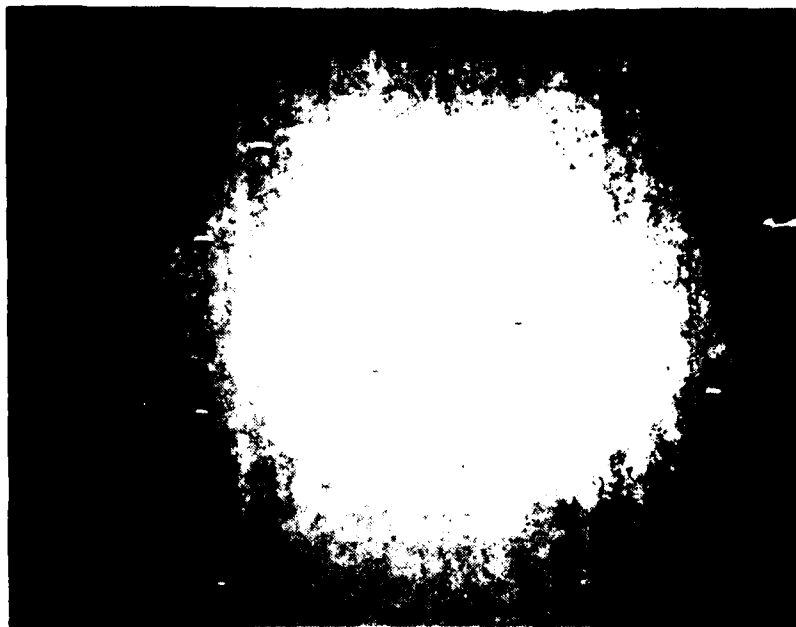


Figure II.1 SEM micrographs of Wright etched defects in a furnace annealed silicon wafer. (Magnification = 460X)



Figure II.2 SEM micrograph of a Wright etched defect in a furnace annealed silicon wafer. (Magnification = 9KX)



Figure 11.3 SEM micrograph of a Wright etched ring of defects in a furnace annealed silicon wafer. (Mag. = 17KX)

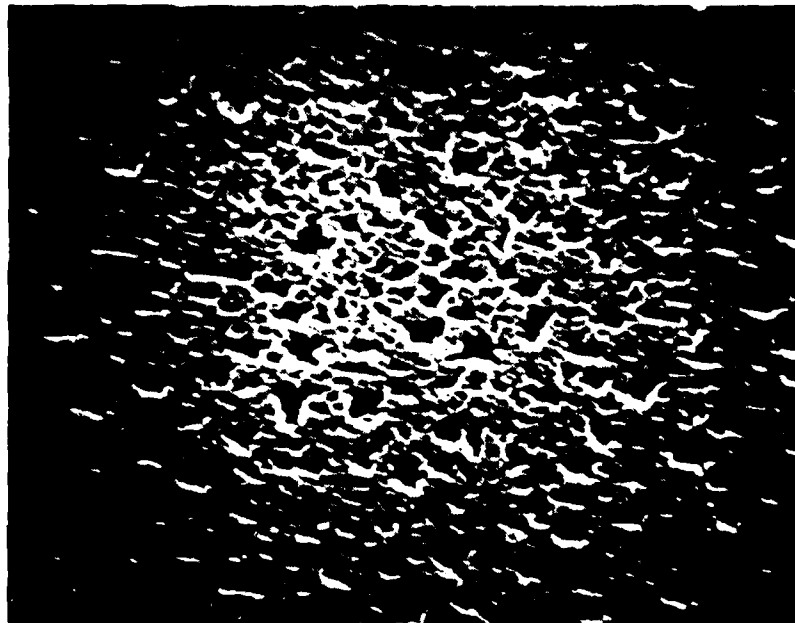


Figure 11.4 SEM micrograph of surface damage to a silicon wafer heated to 1200°C by simulated multiscan annealing. (Mag. = 10KX)

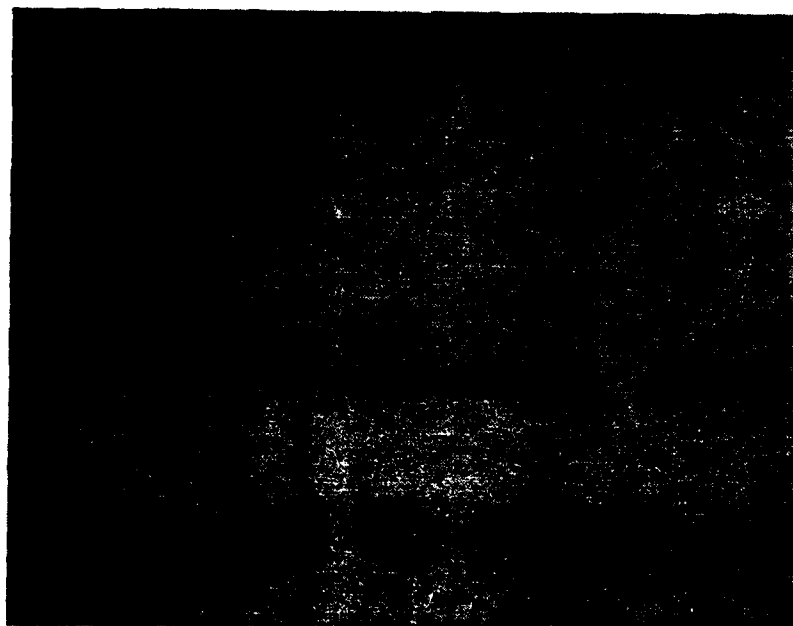


Figure II.5 Optical micrograph of Wright etched defects in a furnace annealed sample. (Mag. = 1KX)




Figure II.6 Optical micrograph of Wright etched defects in a furnace annealed sample which was subsequently annealed by the simulated multiscan method. (Mag. = 1KX)

III. Preliminary Studies of Oxide Densification on Silicon Wafers Annealed by the Simulated Multiscan Method

We studied the possibility of densification of CVD deposited (Silox) oxide by simulated multiscan annealing. The results show clearly that oxide could be densified by this method.

Wafers were obtained which had been coated with 1 μm of silox. Samples annealed at 950°C in N_2 for 1 hour in a conventional furnace were also obtained as a reference. The etch rate of the oxide in 50:1 mixture of water and hydrofluoric acid was taken as a measure of oxide quality. The etch rate of undensified silox was found to be 3000 $\overset{\circ}{\text{A}}$ /minute. The etch rate of furnace annealed samples was 700 $\overset{\circ}{\text{A}}$ /minute.

The undensified samples were heated for 2 minutes in the carbon strip furnace described in Section II at various temperatures. The etch rate is shown in Figure III.1 as a function of the anneal temperature. It is clear from this graph that oxide quality equal to that of the furnace annealed control can be attained.

We conclude that oxide densification can be performed in this annealing regime.

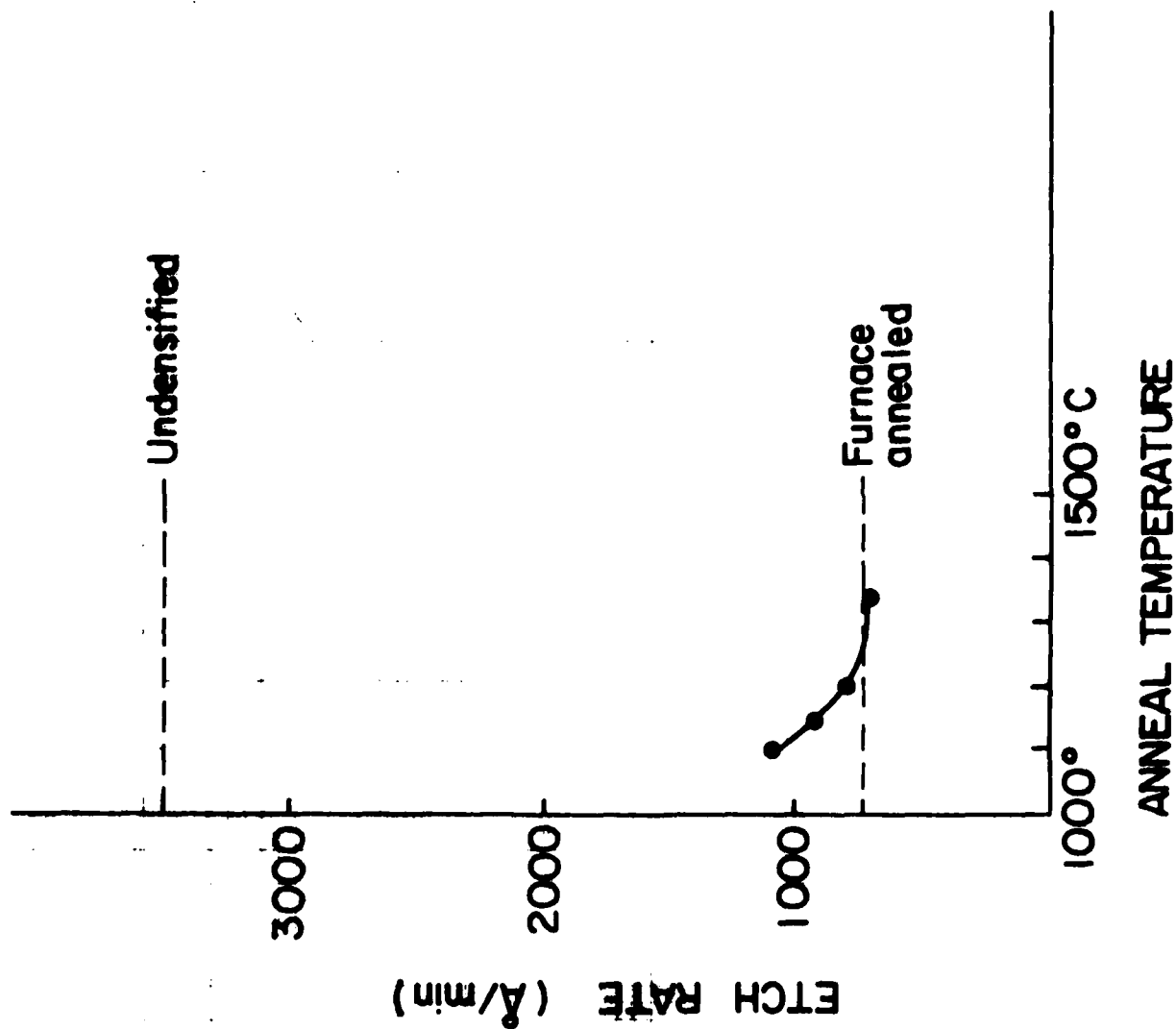


Figure III.1 Etch rate versus anneal temperature for simulated multiscan annealed CVD deposited oxide (Silox).

IV. Stress in WSi_2 /Polysilicon/Oxide Films on Silicon Wafers

IV.0 Abstract

Stress in WSi_2 /Polysilicon/Oxide films on silicon wafers was measured by the optical lever method developed by Bell Laboratories. Stress was found to be very low as compared to other published silicide results, typical values being on the order of 10^9 dynes/cm². These values are close to the detection limit of the method. This limitation is due to nonhomogeneities of the elastic properties and dimensions of the wafers themselves. As a result no clear conclusion could be drawn as to the effect of process parameters on film stress.

IV.A Introduction

Currently, there is an increased interest in silicon wafer stress. The effects of stress on band structure which limits electron mobility (2); the effects of stress on topology which limits lithographic processing (1 and 4); and the stress-induced defects (i.e. cracking) which then relieve the stress but lower the yield (2 and 3) are the reasons which reflect why this analysis was undertaken.

Three popular methods of measuring stress are the laser lever (3), x-ray diffraction (2), and Raman scattering (2). The different methods vary in their resolution, sensitivity, and ease in measurement. The laser lever is the simplest method providing a resolution of approximately 1 cm. Raman scattering has the highest resolution and sensitivity. The resolution for Raman scattering is on the order of 10 μm and for x-ray diffraction is on the order of several mm.

IV.B Experimental

The investigation into the effects of processing parameters on stress in silicon wafers was conducted jointly with a major semiconductor manufacturer. Stress and curvature measurements were performed on 4 inch diameter silicon wafers. The effects of annealing time and temperature on wafer stress were analyzed. Nine wafers were divided into time and temperature sequences. The wafer annealing process with dry nitrogen varied between 850°C to 1000°C and from 15 to 60 minutes. The wafer substrate thickness was 508 μm and the film thicknesses were: WSi_2 , .35 μm ; Poly-silicon, .25 μm ; SiO_2 , .1 μm .

Curvature measurements were obtained with the optical lever shown in Figure IV.1. The wafer translation under the laser beam caused the reflected beam to travel along the wall. This travel varied as a function of the wafer profile.

The simplified geometry of Figure IV.2 is used to simplify the mathematical analysis. By considering the wafer as a rotating mirror and the distance L as a circle radius, the analysis proceeds as follows:

$$\Delta D = L \sin 2\Delta \frac{dy}{dx}$$

where ΔD = arc length

$$\Delta \frac{dy}{dx} = \text{mirror rotation angle}$$

$$2\Delta \frac{dy}{dx} = \text{reflected beam variance angle}$$

$$\sin^2 \Delta \frac{dy}{dx} = 2\Delta \frac{dy}{dx} \text{ for small variance}$$

$$\text{Therefore } \Delta D = 2LD \frac{dy}{dx} = 2L\Delta \frac{dy}{dx} \frac{\Delta x}{\Delta x} = 2L \frac{d^2y}{dx^2} \Delta x \quad (1)$$

For a circle

$$x^2 + y^2 = R^2 \quad y = (R^2 - x^2)^{1/2}$$

$$dy/dx = -x(R^2 - x^2)^{-1/2} \approx -x/R \quad \text{for } x \ll R$$

$$d^2y/dx^2 = -R^2(R^2 - x^2)^{-3/2} \approx -1/R \quad \text{for } x \ll R$$

Substituting the above derivatives into Equation (1) yields

$$\Delta D = \frac{2LDX}{R} \quad \text{or} \quad R = \frac{2LDX}{\Delta D} \quad (2)$$

For our purposes, the rotating mirror is replaced by a traveling wafer where the surface curvature creates the angle deviations. ΔX is now the wafer translation, L is the distance traveled by the reflected beam, ΔD is the resulting translation of the reflected beam, and R is the wafer radius of curvature. The film stress can then be calculated once R is known as shown by Sinha.

$$\sigma = \frac{ED^2}{6(1-\nu)Rt} = \frac{2 \cdot 10^{12}}{6Rt} D^2 \quad \text{for Si wafers} \quad (3)$$

where

σ = stress in dynes cm^{-2}

R = wafer radius of curvature cm

D = substrate thickness cm

t = film thickness cm

To test for consistency in our results, one wafer was cracked along its main axis to determine the relation between stress and wafer size and shape. The average stress in the wafer did not vary after cracking. This consistency proved that wafer stress was independent of size and shape.

IV.C Results

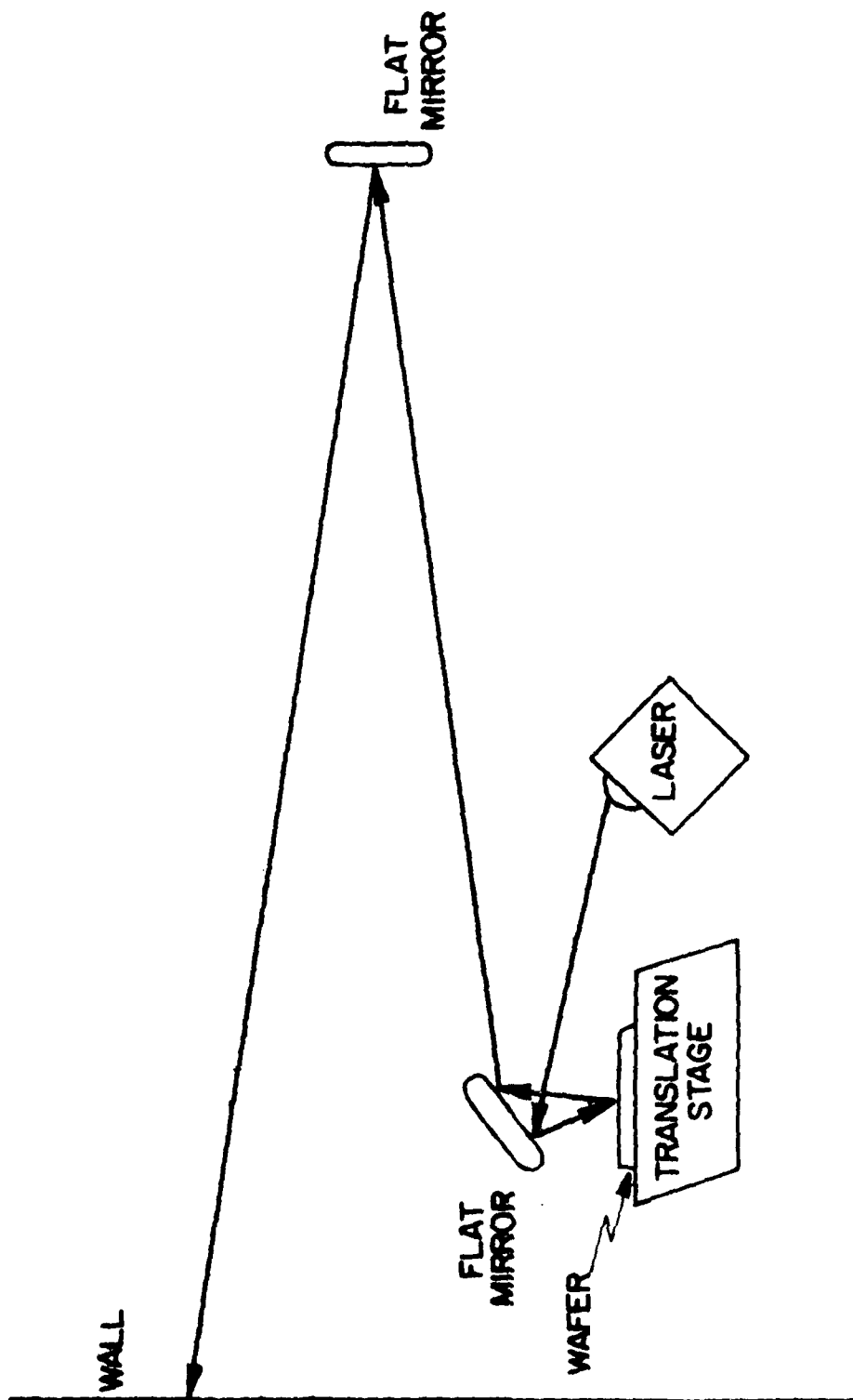
Curvature measurements were obtained at 1/2" intervals along the two (100) wafer axes as shown in Figure IV.3. The mean stress and the standard deviations of the measured stress about the mean were obtained for each wafer. The relation between stress and annealing temperature is shown in Figure IV.4 for 30 minute anneal time. Figures IV.5 and IV.6 show the dependence of stress on anneal time for temperatures of 975°C and 1000°C, respectively. It is clear that the standard deviations are so large that meaningful trends cannot be extracted from the data. The stress is so small that the usefulness of the wafer as a strain gage is very limited. This problem of sensitivity can probably be alleviated by using 3" wafers (which are much thinner than 4" wafers).

IV.D Discussion of the Bell Labs Method of Stress Measurement

The measurement of curvature gives a macroscopic average indication of film stress which may not be relevant for microcircuit fabrication. As Gegenworth (5) has forcefully emphasized, the Bell Labs method ignores microscopic deformation of the wafer which can be caused by film stress or other process related effects, such as non-uniform heating and cooling. These deformations occur on the .1 - 1 μ m scale and may have catastrophic effects on yields. Moreover, they may cause a discrepancy between the true microscopic stress and the macroscopic stress measured by the Bell Labs technique.

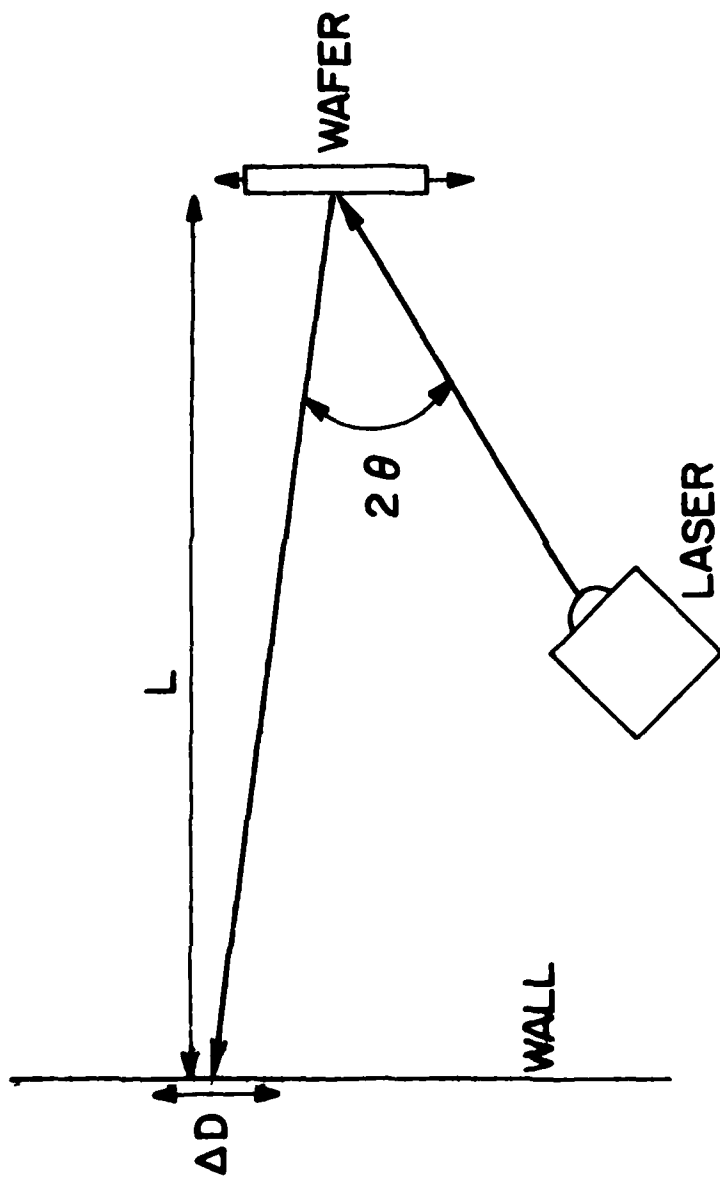
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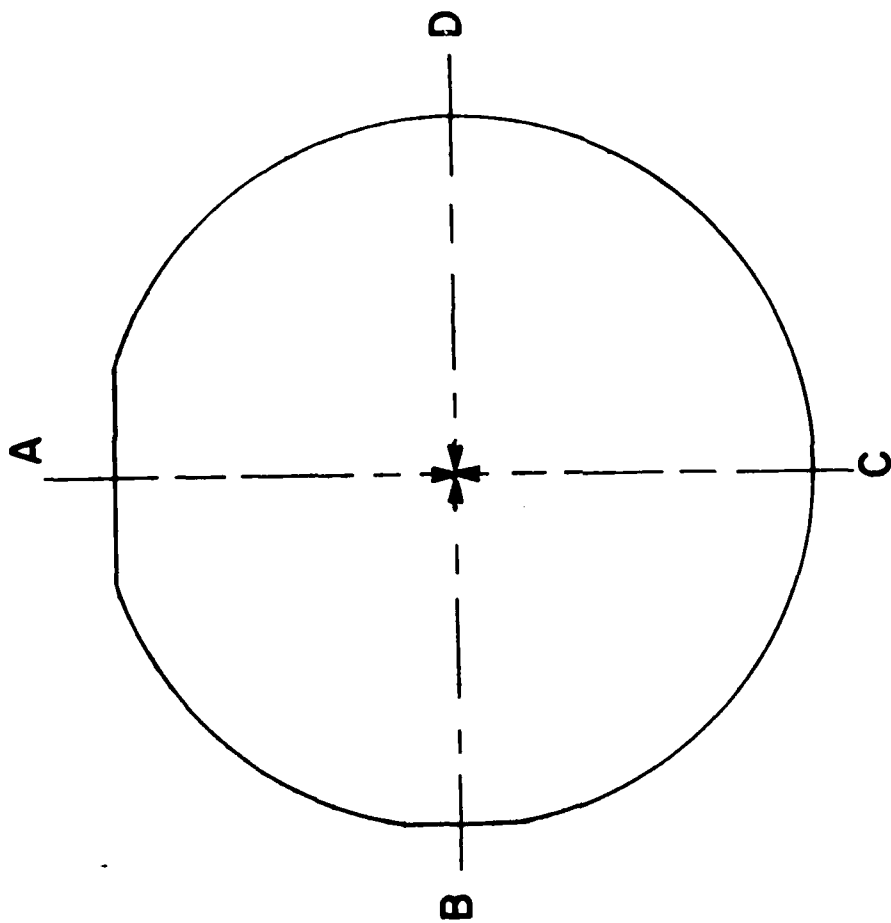
ACTUAL GEOMETRY OF LASER LEVER APPARATUS

Figure IV.1 Laser lever apparatus.



SIMPLIFIED VIEW OF LASER LEVER APPARATUS

Figure IV.2 Simplified view of laser lever apparatus.



MEASUREMENT AXES

Figure IV.3 Measurement axes for stress measurements on 100 silicon wafers.

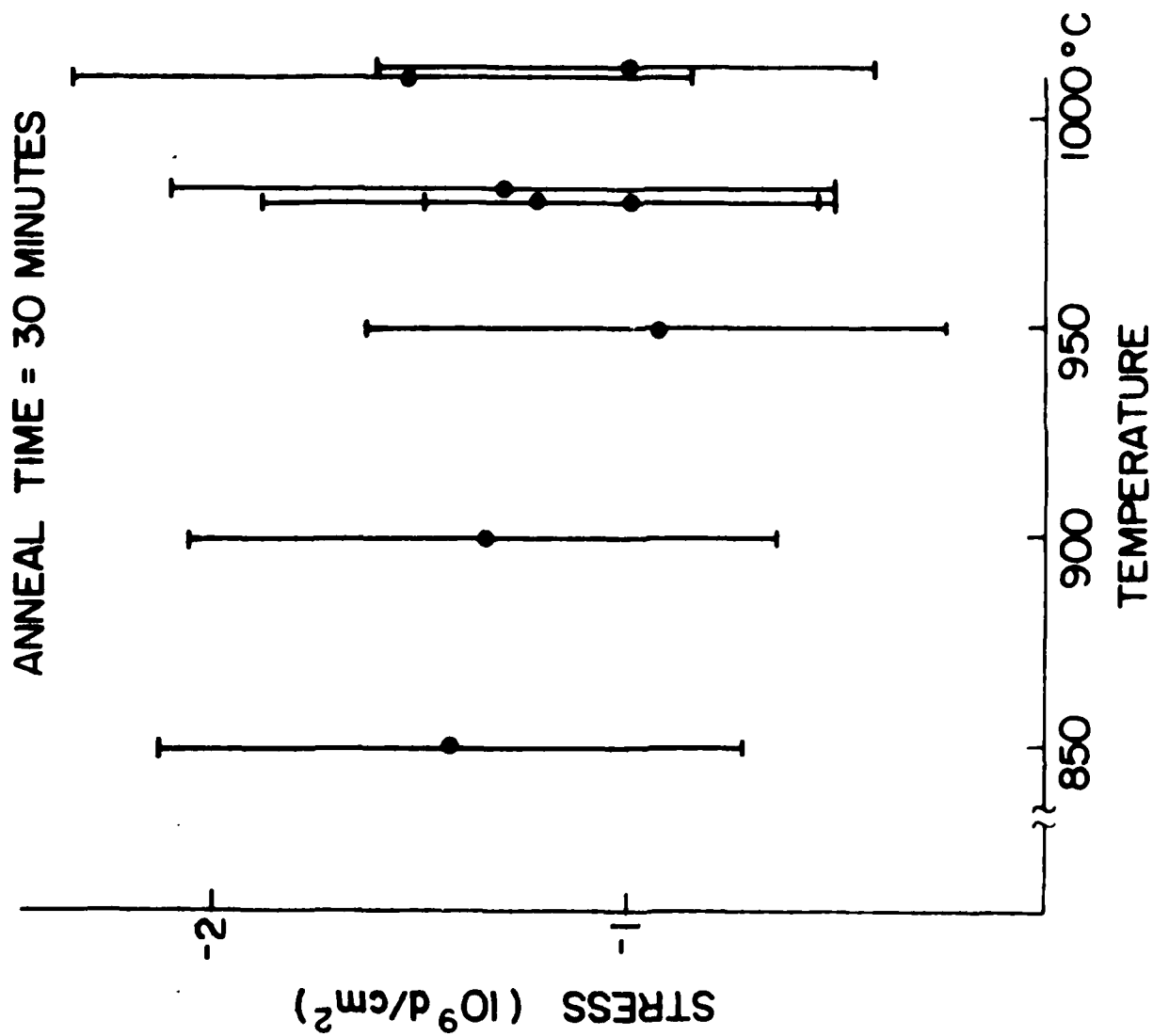


Figure 10. Stress versus anneal temperature for a 30 minute anneal.

ANNEAL TEMPERATURE = 975°C

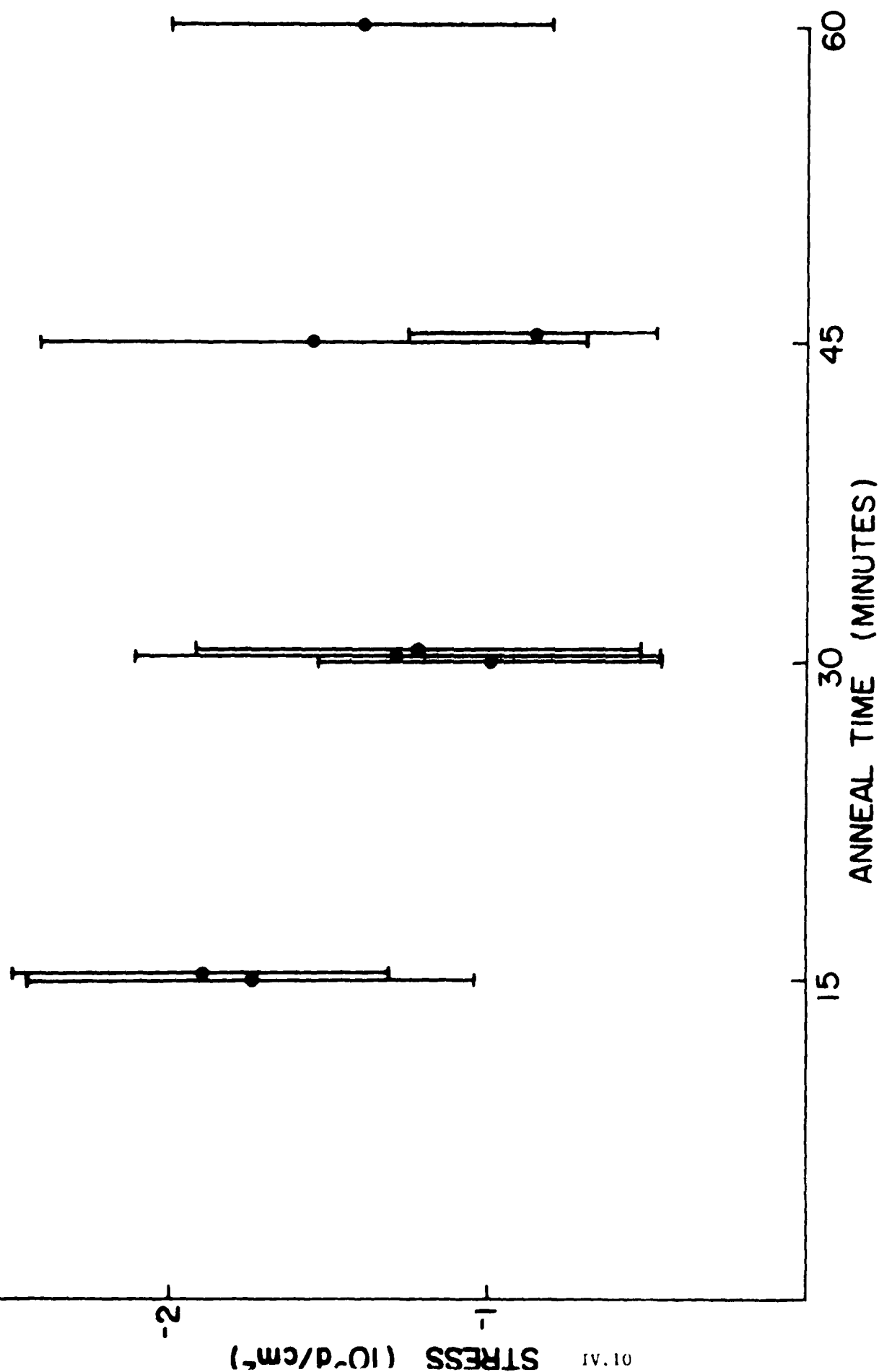


Figure IV.1 Stress versus anneal time for 970°C anneal temperature.

ANNEAL TEMPERATURE = 1000°C

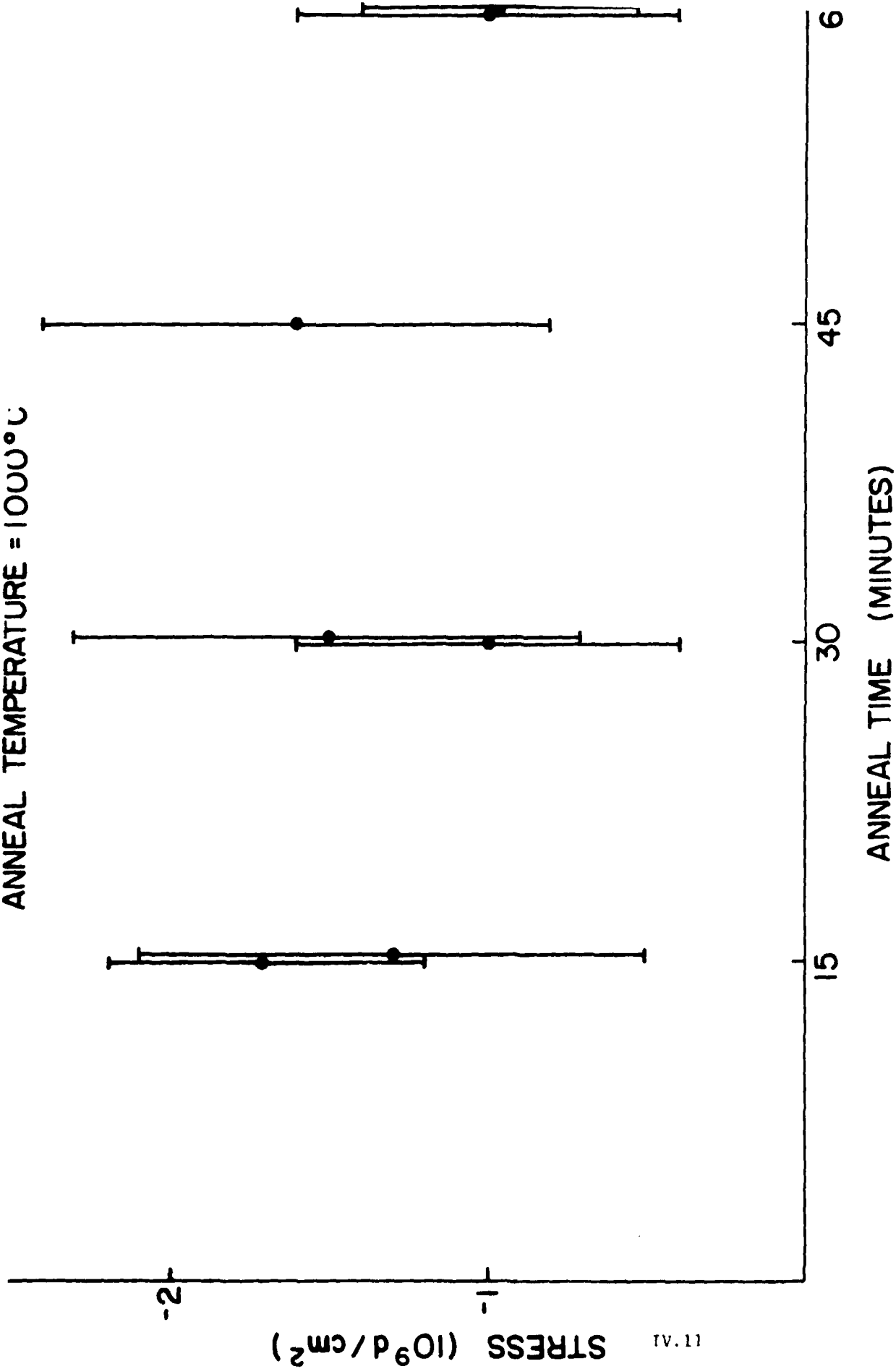


Figure IV.6 Stress versus anneal time for 1000°C anneal temperature.

V. Analysis of an Electron Beam Source for Full Water Annealing

We have seen that the simulated multiscan annealing method is capable of wafer damage removal and oxide densification. This, together with the evidence of McMahon and Ahmed (1) on device structures, suggests that an electron source capable of uniform, controlled heating of silicon wafers to temperatures near the melting point in a few seconds could be extremely valuable. The machine should however be simpler and cheaper than Ahmed's modified scanning electron microscope type of machine. The thin film field emitter arrays developed by Stanford Research Institute appear to be ideal for this purpose, even though the technology has not yet produced devices of sufficient reliability to use at this time. We feel that the analysis presented below shows these devices so appropriate for the application that intensified efforts to improve the technology are warranted.

The integrated field emitter structure and performance have been described by Spindt et. al. (1). We propose that a simple annealing machine be constructed along the lines of Figure V.1. The low voltage electrons emitted from a large area emitter are accelerated by a high potential between the wafer and the gate electrode of the emitter array. The absence of focusing and deflection represent a significant simplification over scanning type machines.

It is easily shown that heating a thermally isolated silicon wafer to the melting point requires about 1 kJ/cm^2 of energy. If this energy is deposited in 10 seconds, 100 W/cm^2 of power is required. If the final accelerating potential is 10 kV, the emission current should be 10 mA/cm^2 . Since emission densities of 10 A/cm^2 have been reported for these structures, the emission requirement for annealing is minimal. Cathode power dissipa-

tion will be very small due to the small voltage required on the gate electrode and the low emission currents. Maximum cathode dissipation should be 1 W/cm^2 . The machine would require about 30 watt-hours of energy per wafer. This is somewhat less than a furnace operated at maximum throughput and 100 times less than that required by a single scan laser system. Moreover, the throughputs would be limited by load/unload times and could approach 100 wafers per hour as opposed to 15 for single scan system.

It therefore seems appropriate to try to improve on the reliability of field emitter arrays for annealing purposes. We are currently studying this problem.

An alternative approach to a full wafer exposure system involves a new LaB_6 cathode (3) developed at the Oregon Graduate Center in a Pierce gun structure. We are studying this design in cooperation with Dr. L. Swanson at the Oregon Graduate Center.

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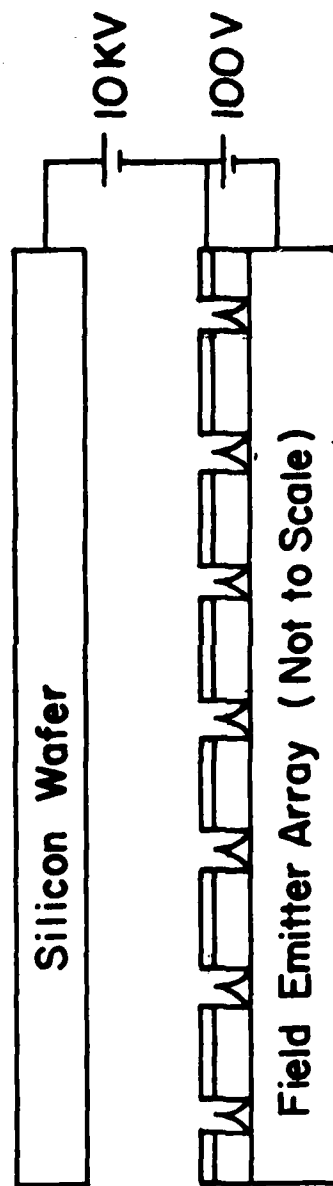


Figure 1-1 Annealing machine using the SRI field emitter array.

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